What is claimed is:

1. In a computerized device, a method for controlling speculative execution of instructions, the method comprising the steps of:

executing a set of instructions on a processor in the computerized device;

detecting a value of a speculation indicator;

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allowing speculative execution of instructions in the processor; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allowing speculative execution of instructions in the processor.

2. The method of claim 1 further comprising the steps of:

setting the value of the speculation indicator to indicate that speculative execution of load instructions is not allowed in the computerized device; and

deactivating at least one speculative execution correction mechanism in the computerized device.

3. The method of claim 2 wherein the processor in the computerized device operates a uniaccess execution environment and wherein the step of deactivating at least one speculative execution correction mechanism in the computerized device comprises the steps of:

deactivating a uniaccess speculative execution correction mechanism; and

deactivating a multiaccess speculative execution correction mechanism.

4. The method of claim 1 further comprising the steps of:

setting the value of the speculation indicator to indicate that speculative execution of load instructions is allowed in the computerized device.

5. The method of claim 4 wherein the processor in the computerized device operates a uniaccess execution environment; and

wherein the step of allowing speculative execution of load instructions in the processor comprises the step of deactivating a multiaccess speculative execution correction mechanism in the computerized device.

6. The method of claim 4, wherein the step of allowing speculative execution of load instructions in the processor comprises the steps of:

speculatively executing a load instruction in the processor;

detecting, at a time after speculatively executing the load instruction, a subsequent instruction which is adversely affected by the step of speculatively executing the load instruction; and

performing a speculative execution recover operation.

7. The method of claim 6 wherein:

the subsequent instruction is a store instruction containing a memory reference related to the speculatively executed load instruction; and

the step of performing a speculative execution recover operation comprises the step of performing a uniaccess speculative execution recover operation.

8. The method of claim 6 wherein the step of speculatively executing a load instruction in the processor includes the steps of:

detecting the load instruction following the subsequent instruction in the set of instructions being executed on the processor; and

executing the load instruction prior to executing the subsequent instruction.

9. The method of claim 6 wherein:

the computerized device operates a multiaccess execution environment;

the step of detecting a subsequent instruction which is adversely affected by the step of speculatively executing the load instruction compromises a step of operating a

multiaccess speculative execution correction mechanism that detects a memory reference by a subsequent instruction in the multiaccess execution environment that is adversely affected by the step of speculatively executing the load instruction; and

the step of performing a speculative execution recover operation comprises the step of performing a multiaccess speculative execution recover operation.

10. The method of claim 1 wherein the processor in the computerized device operates a multiaccess execution environment and wherein the method further comprises the step of:

if a process containing the set of instructions does not contain a shared memory condition then setting the value of the speculation indicator to indicate that speculative execution of load instructions is allowed in the computerized device.

11. The method of claim 1 wherein the step of detecting a value of a speculation indicator comprises the step of:

consulting the speculation indicator in a processor control register associated with the processor in the computerized device to determine the value of the speculation indicator.

12. The method of claim 1 wherein the step of detecting a value of a speculation indicator comprises the step of:

consulting the speculation indicator in a page table associated with the set of instructions executing on the processor in the computerized device.

13. The method of claim 1 wherein the step of executing a set of instructions on a processor in the computerized device comprises the steps of:

executing a set speculation indicator instruction within the set of instructions on the processor to set the value of the speculation indicator.

14. The method of claim 1 wherein the speculation indicator includes a plurality of speculative indicator storage locations each capable of maintaining a respective

speculative indicator value and wherein the step of detecting a value of the speculation indicator comprises the steps of:

obtaining respective speculative indicator values from certain of the plurality of speculative indicator storage locations; and

processing the respective speculative indicator values according to a speculative execution policy to determine the value of the speculation indicator.

15. A processor configured to control speculative execution of load instructions, the processor comprising:

an instruction orderer configured to receive and order a set of instructions for execution;

an instruction executer coupled to the instruction orderer, the instruction executer configured to execute instructions in the set of instructions according to an order indicated by the instruction orderer;

a speculation indicator configured to receive and maintain a value that indicates if speculative execution of instructions is allowed in the processor; and

a speculative execution controller coupled to at least one of the instruction orderer and the instruction executer and coupled to the speculation indicator, the speculative execution controller configured to detect the value of a speculation indicator and configured to allow speculative execution of instructions in the processor if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the processor, and configured to not allow speculative execution of instructions in the processor if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the processor.

16. The processor of claim 15 further wherein:

at least one of the instruction executer and the speculative execution controller is configured to set the value of the speculation indicator to indicate that speculative execution of load instructions is not allowed in the processor; and

wherein the speculative execution controller is configured to deactivate at least one speculative execution correction mechanism coupled to the instruction executer.

17. The processor of claim 16 wherein:

the processor is configured to operate a uniaccess execution environment; and

wherein the speculative execution controller is configured to deactivate a uniaccess speculative execution correction mechanism and is configured to deactivate a multiaccess speculative execution correction mechanism.

18. The processor of claim 15 wherein at least one of the instruction executer and the speculative execution controller is configured to set the value of the speculation indicator to indicate that speculative execution of load instructions is allowed in the processor.

19. The processor of claim 18 wherein:

the processor is configured to operate a uniaccess execution environment; and

wherein the speculative execution controller is configured to deactivate a multiaccess speculative execution correction mechanism in the computerized device.

20. The processor of claim 18 wherein when the speculative execution controller is configured to allow speculative execution of load instructions in the processor:

the instruction order is configured to speculatively reorder a load instruction and the instruction executer is configured to speculatively execute the load instruction;

the speculative execution correction mechanism is configured to detect, at a time after the instruction executer speculatively executes the load instruction, a subsequent instruction which is adversely affected by speculatively executing the load instruction; and

the speculative execution correction mechanism is configured to perform a speculative execution recover operation.

21. The processor of claim 20 wherein:

the subsequent instruction is a store instruction containing a memory reference related to the speculatively executed load instruction; and

wherein the speculative execution correction mechanism is configured to perform a uniaccess speculative execution recover operation.

22. The processor of claim 20 wherein:

the instruction orderer is configured to detect the load instruction following the subsequent instruction in a set of instructions being executed on the processor and is configured to reorder the load instruction prior to the subsequent instruction; and

wherein the instruction executer is configured to execute the load instruction prior to executing the subsequent instruction.

23. The processor of claim 20 wherein:

the processor is configured to operate in a multiaccess execution environment;

the speculative execution correction mechanism is a multiaccess speculative execution correction mechanism configured to detect a memory reference by a subsequent instruction in the multiaccess execution environment that is adversely affected by the instruction executer speculatively executing the load instruction; and

the multiaccess speculative execution correction mechanism is configured to perform a multiaccess speculative execution recover operation.

24. The processor of claim 15 wherein:

the processor is configured to operate a multiaccess execution environment; and

at least one of the instruction executer and the speculative execution controller are configured to determine if a process does not contain a shared memory condition then to set the value of the speculation indicator to indicate that speculative execution of load instructions is allowed in the computerized device.

25. The processor of claim 15 wherein:

the speculation indicator is contained in a processor control register associated with the processor; and

the speculative execution controller is coupled to the processor control register to detect the value of the speculation indicator.

26. The processor of claim 15 wherein:

the speculation indicator is contained in a page table associated with the set of instructions; and

the speculative execution controller is configured to detect the value of the speculation indicator from the page table.

27. The processor of claim 15 wherein:

at least one of the instruction executer and the speculative execution controller are configured to detect a set speculation indicator instruction within the set of instructions on the processor and are configured to set the value of the speculation indicator based on the set speculation indicator instruction.

28. A processor configured to control speculative execution of load instructions, the processor comprising:

an instruction orderer configured with means for receiving and ordering a set of instructions for execution;

an instruction executer coupled to the instruction orderer, the instruction executer configured with means for executing instructions in the set of instructions according to an order indicated by the instruction orderer;

a speculation indicator configured to receive and maintain a value that indicates if speculative execution is allowed of instructions is allowed in the processor; and

a speculative execution controller coupled to at least one of the instruction orderer and the instruction executer and coupled to the speculation indicator, the speculative execution controller configured with means for detecting the value of a speculation indicator and for allowing speculative execution of instructions in the processor if the

value of the speculation indicator indicates that speculative execution of instructions is allowed in the processor, and for not allowing speculative execution of instructions in the processor if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the processor.

29. A computer program product having a computer-readable medium including computer program logic encoded thereon that, when performed in a computer device having a coupling of a memory and a processor, programs the processor to perform the operations of:

execute a set of instructions in the computerized device;

detect a value of a speculation indicator;

if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device, allow speculative execution of instructions; and

if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device, not allow speculative execution of instructions.